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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,981	09/05/2006	John Kouvetakis	05-720-US2	6588

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EXAMINER	
PATEL, REEMA	
ART UNIT	**PAPER NUMBER**
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/559,981	KOUVETAKIS ET AL.	
	Examiner	Art Unit	
	Reema Patel	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) was submitted on 12/20/06. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by He et al. (U.S. 6,037,614).

4. Regarding claim 1, He et al. discloses a semiconductor structure comprising: a substrate and a Sn_xGe_{1-x} layer formed over the substrate, wherein x has a value from about 0.02 to about 0.20 (col 5, lines 42-44).

5. Regarding claim 2, He et al. discloses the Sn_xGe_{1-x} layer is an epitaxial layer with a direct band gap between about 0.72eV and about .041eV (col 10, lines 53-55).

6. Regarding claim 3, He et al. discloses x has a value of about 0.20 (col 6, lines 9-10) and the Sn_xGe_{1-x} layer is a direct-gap material (col 10, lines 53-55).

7. Regarding claim 4, He et al. discloses the substrate comprises a silicon substrate (col 5, lines 24-25, 46-47).

8. Regarding claim 5, He et al. discloses the substrate comprises Si(100) (col 5, lines 24-25, 46-47).

9. Regarding claim 10, He et al. discloses the Sn_xGe_{1-x} layer has a thickness from about 50nm to about 1000nm (col 6, lines 51-52).

10. Claims 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Soref et al. (U.S. 5,548,128).

11. Regarding claim 13, Soref et al. discloses a semiconductor comprising a Ge-Sn quantum structure formed over a silicon substrate (col 2, lines 45-47).

12. Regarding claim 14, Soref et al. discloses the Ge-Sn quantum structure comprises $Ge_{1-x}Sn_x$ and x has a value from about 0.02 to about 0.03 (col 2, lines 59-61).

13. Regarding claim 15, Soref et al. discloses the Ge-Sn quantum structure is formed over Ge-Sn epitaxial layer formed over the silicon substrate (col 3, lines 27-29).

14. Claims 1 and 7-8 are rejected under 35 U.S.C. 102(a) as being anticipated by Bauer et al. ("Ge-Sn semiconductors for band-gap and lattice engineering").

15. Regarding claim 1, Bauer et al. discloses a semiconductor structure comprising: a substrate and a Sn_xGe_{1-x} layer formed over the substrate, wherein x has a value from about 0.02 to about 0.20 (page 2992, col 1, lines 27-28).

16. Regarding claim 7, Bauer et al. discloses the substrate comprises a silicon substrate and the Sn_xGe_{1-x} layer is formed directly on the substrate (page 2992, col 1, lines 27-28).

17. Regarding claim 8, Bauer et al. discloses that the substrate comprises Si(100) (page 2992, col 1, lines 27-28).

18. Claims 17-23 rejected under 35 U.S.C. 102(a) as being anticipated by Bauer et al. ("Tunable band structure in diamond-cubic tin-germanium alloys grown on silicon substrates").

19. Regarding claim 17, Bauer et al. discloses a method for depositing an epitaxial Ge-Sn layer on a substrate in a chemical vapor deposition reaction chamber, the method comprising introducing into the chamber a gaseous precursor comprising SnD_4 under conditions whereby the epitaxial Ge-Sn layer is formed on the substrate (page 356, col 1, lines 39-42).

20. Regarding claim 18, Bauer et al. discloses the gaseous precursor comprises SnD_4 and high purity H_2 (page 356, col 1, lines 39-42).

21. Regarding claim 19, Bauer et al. discloses the gaseous-precursor, comprises high purity H_2 of about 15-20% by volume (page 356, col 1, lines 39-42).

22. Regarding claim 20, Bauer et al. discloses the gaseous precursor is introduced at a temperature in a range of about 250°C to about 350°C (page 356, col 1, lines 45-48).

23. Regarding claim 21, Bauer et al. discloses the substrate comprises silicon (page 356, col 1, lines 45-46).

24. Regarding claim 22, Bauer et al. discloses the silicon comprises Si(100) (page 356, col 1, lines 45-46).

25. Regarding claim 23, Bauer et al. discloses the Ge-Sn layer comprises $Ge_{1-x}Sn_x$ and x is in a range from about .02 to about .20 (page 356, col 1, lines 54-55).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al. ("Ge-Sn semiconductors for band-gap and lattice engineering") in view of Bader et al. (U.S. 6,849,878 B2).

28. Regarding claim 9, Bauer et al. discloses the limitations of claim 7 and discloses the use of a Si(100) substrate but does not disclose the use of a Si(111) substrate. However, Bader et al. (U.S. 6,849,878 B2) discloses that it is preferable to use a Si(111) substrate because such substrates are easy to machine and prepare for epitaxy (col 3, lines 55-59). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Bauer et al. with using a Si(111) substrate, as taught by Bader et al., so as to ease the process of machining and preparing the substrate.

29. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (U.S. 6,037,614) as applied to claim 1 above, and further in view of Soref et al. (U.S. 5,548,128).

30. Regarding claim 11, He et al. discloses the limitations of claim 1 but does not disclose forming a strained Ge layer over the Sn_xGe_{1-x} layer. However, Soref et al. discloses forming a strained Ge layer over a Sn_xGe_{1-x} layer (col 2, lines 47-49, 59-77) for the purpose of producing a multiple quantum well stack which has superior infrared light manipulation abilities (col 1, lines 54-56). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of He et al. with forming a strained Ge layer over a Sn_xGe_{1-x} layer so as to produce a multiple quantum well stack which has superior infrared light manipulation abilities.

31. Regarding claim 12, Soref et al. discloses that x is greater than about 0.11 and the strained Ge layer is a direct-gap material (col 2, lines 59-67).

32. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soref et al. (U.S. 5,548,128) as applied to claim 13 above, and further in view of Yamauchi et al. (2003/0219933 A1).

33. Regarding claim 16, Soref et al. discloses the limitations of claim 13 and the use of a silicon substrate but does not disclose that the substrate comprises Si(100). However, Yamauchi et al. discloses that the use of an Si(100) substrate is desirable because an epitaxially grown film formed over such a substrate has a better

crystallographic structure as compared to those films formed on other types of substrates ([0083]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Soref et al. with the use of an Si(100) substrate so as to form an epitaxially grown film with better crystallographic structure.

34. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al. ("Ge-Sn semiconductors for band-gap and lattice engineering") in view of Soref et al. (U.S. 5,548,128).

35. Regarding claim 24, Bauer et al. discloses introducing into a chamber a combination comprising SnD_4 and Ge_2H_6 under conditions whereby the Ge-Sn layer is formed on the substrate (page 2992, col 2, lines 6-7).

36. Yet, Bauer et al. does not disclose a Ge layer formed on the Ge-Sn buffer layer. However, Soref et al. discloses forming a strained Ge layer over a Sn_xGe_{1-x} layer (col 2, lines 47-49, 59-77) for the purpose of producing a multiple quantum well stack which has superior infrared light manipulation abilities (col 1, lines 54-56). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the layer forming method of Bauer et al. with forming a strained Ge layer over a Sn_xGe_{1-x} layer, as taught by Soref et al., so as to produce a multiple quantum well stack which has superior infrared light manipulation abilities.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RSP
4/19/07

SCOTT B. GEYER
PRIMARY EXAMINER

SBG 4/25/07